DATA SHEET

TDA8561Q
2 × 24 W BTL or 4 × 12 W single-ended car radio power amplifier

Product specification
Supersedes data of July 1994
File under Integrated Circuits, IC01

1997 Sep 22

Philips
Semiconductors





2 × 24 W BTL or 4 × 12 W single-ended car radio power amplifier

TDA8561Q

FEATURES

- Requires very few external components
- High output power
- Flexibility in use; Quad single-ended or stereo BTL
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA8561Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) power package. It contains 4 × 12 W Single-Ended (SE) or 2 × 24 W Bridge-Tied Load (BTL) amplifiers.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	standby current		–	0.1	100	μA
Stereo BTL application						
P_o	output power	$R_L = 4\ \Omega$; THD = 10%	–	24	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	$R_s = 0\ \Omega$	–	70	–	μV
$\|Z_I\|$	input impedance		25	–	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
Quad single-ended application						
P_o	output power	THD = 10%				
		$R_L = 4\ \Omega$	–	7	–	W
		$R_L = 2\ \Omega$	–	12	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	$R_s = 0\ \Omega$	–	50	–	μV
$\|Z_I\|$	input impedance		50	–	–	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8561Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

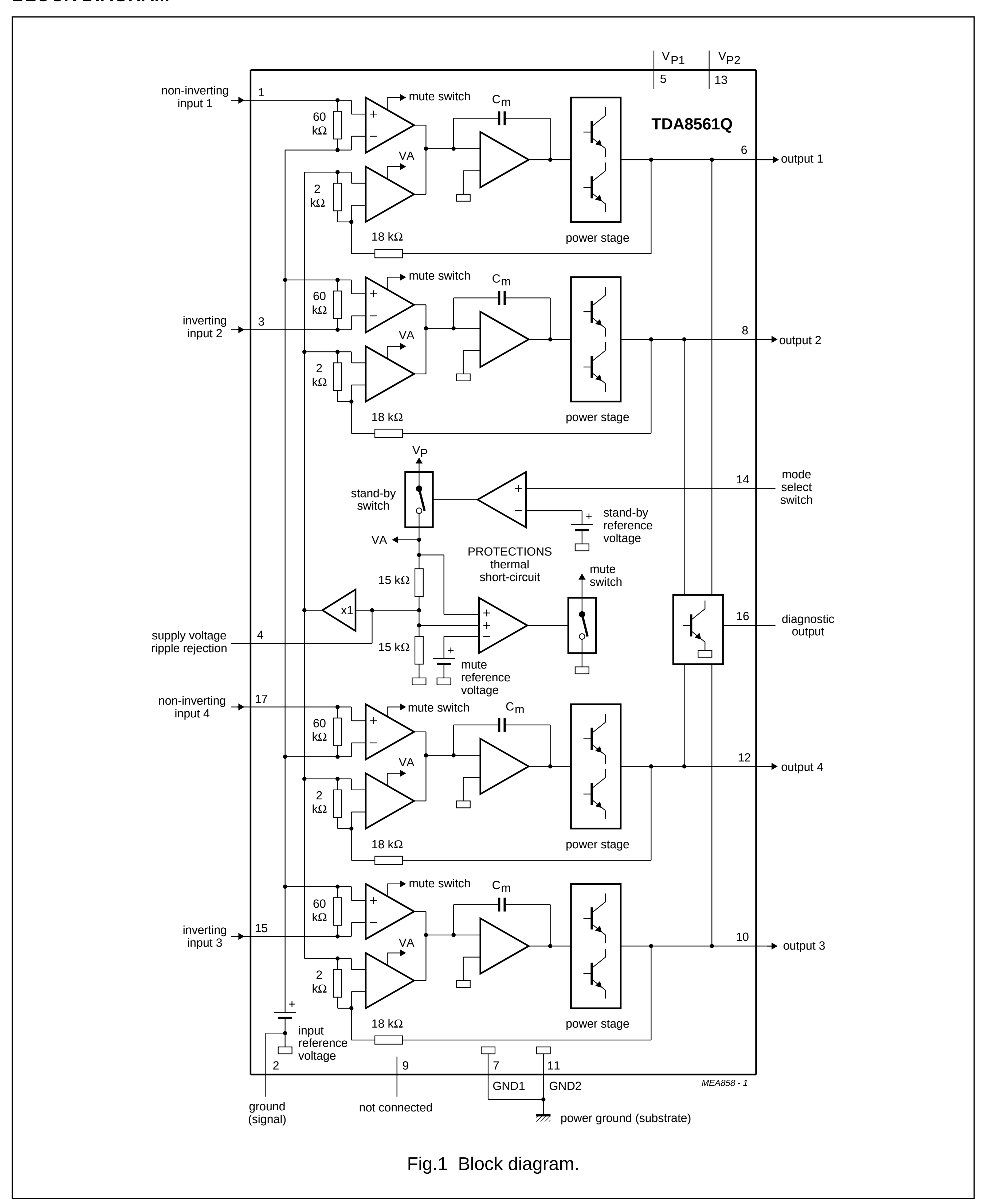


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV 1	1	non-inverting input 1
GND(S)	2	signal ground
INV 2	3	inverting input 2
RR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage
OUT 1	6	output 1
GND1	7	power ground 1
OUT 2	8	output 2
n.c.	9	not connected
OUT 3	10	output 3
GND2	11	power ground 2
OUT 4	12	output 4
V_{P2}	13	supply voltage
MODE	14	mode select switch input
INV 3	15	inverting input 3
V_{DIAG}	16	diagnostic output
–INV 4	17	non-inverting input 4

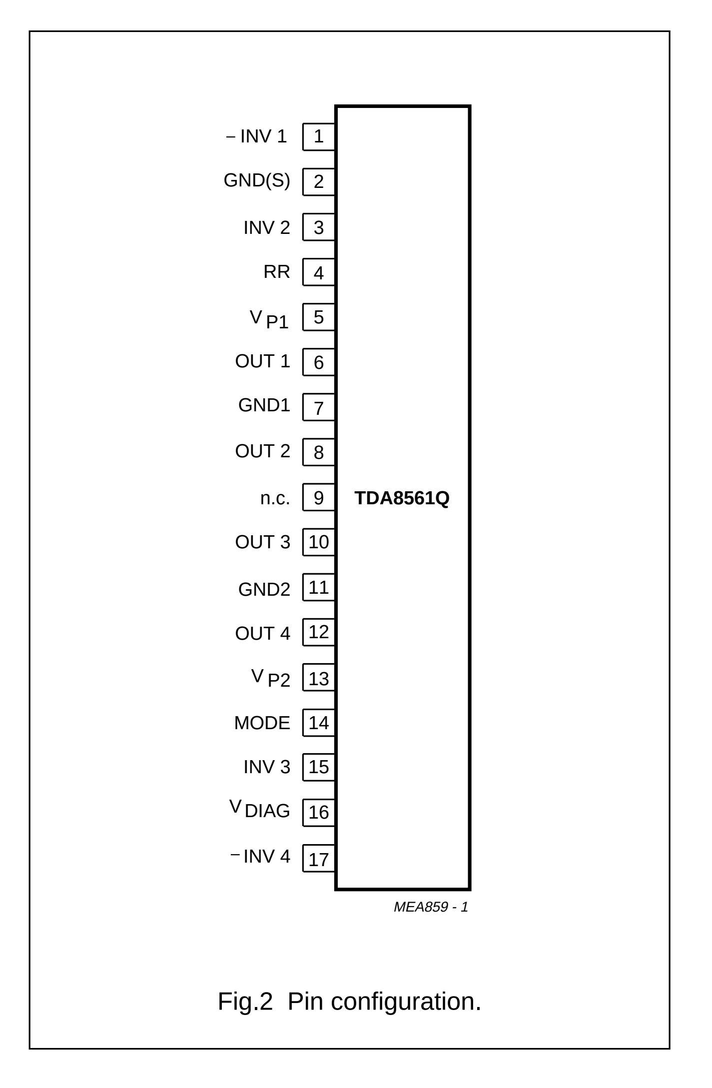


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8561Q contains four identical amplifiers and can be used for Single-Ended (SE) or Bridge-Tied Load (BTL) applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). Special features of the device are:

Mode select switch (pin 14)

- Low standby current (<100 μA)
- Low switching current (low cost supply switch)
- Mute facility.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥100 ms (charging of the input capacitors at pins 1, 3, 15 and 17). This can be achieved by:

- Microcontroller control
- External timing circuit (see Fig.11).

Diagnostic output (pin 16)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 16 goes LOW. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 16 is independent of the number of channels that are clipping (see Figs 3 and 4).

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms, after removal of the short-circuit. During this short-circuit condition, pin 16 is continuously LOW.

When a short-circuit across the load of one or both channels occurs the output stages are switched off for approximately 20 ms. After that time it is checked during approximately 50 μs to see whether the short-circuit is still present. Due to this duty cycle of 50 μs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).

During this short-circuit condition, pin 16 is LOW for 20 ms and HIGH for 50 μs (see Fig.5).

The power dissipation in any short-circuit condition is very low.

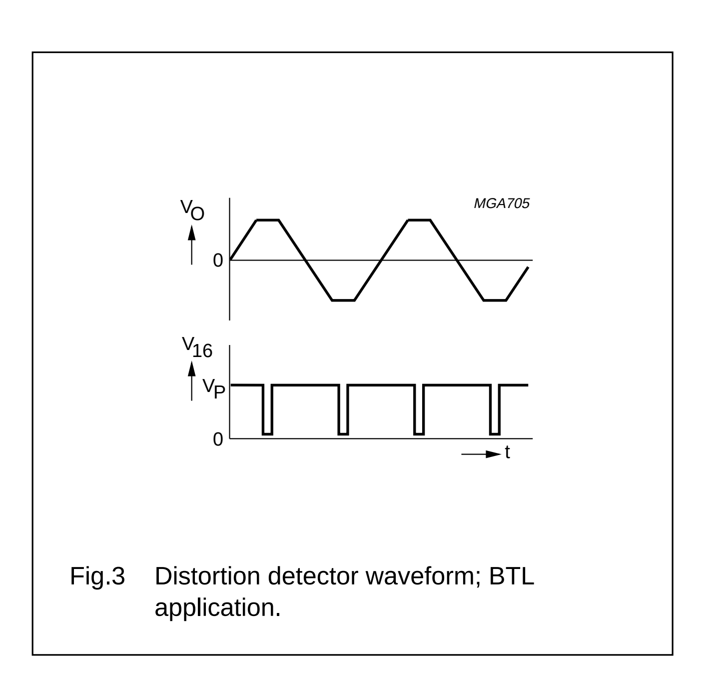


Fig.3 Distortion detector waveform; BTL application.

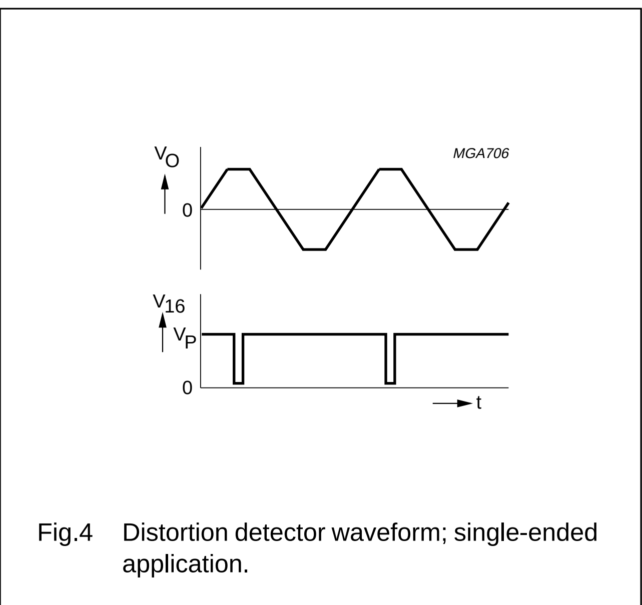


Fig.4 Distortion detector waveform; single-ended application.

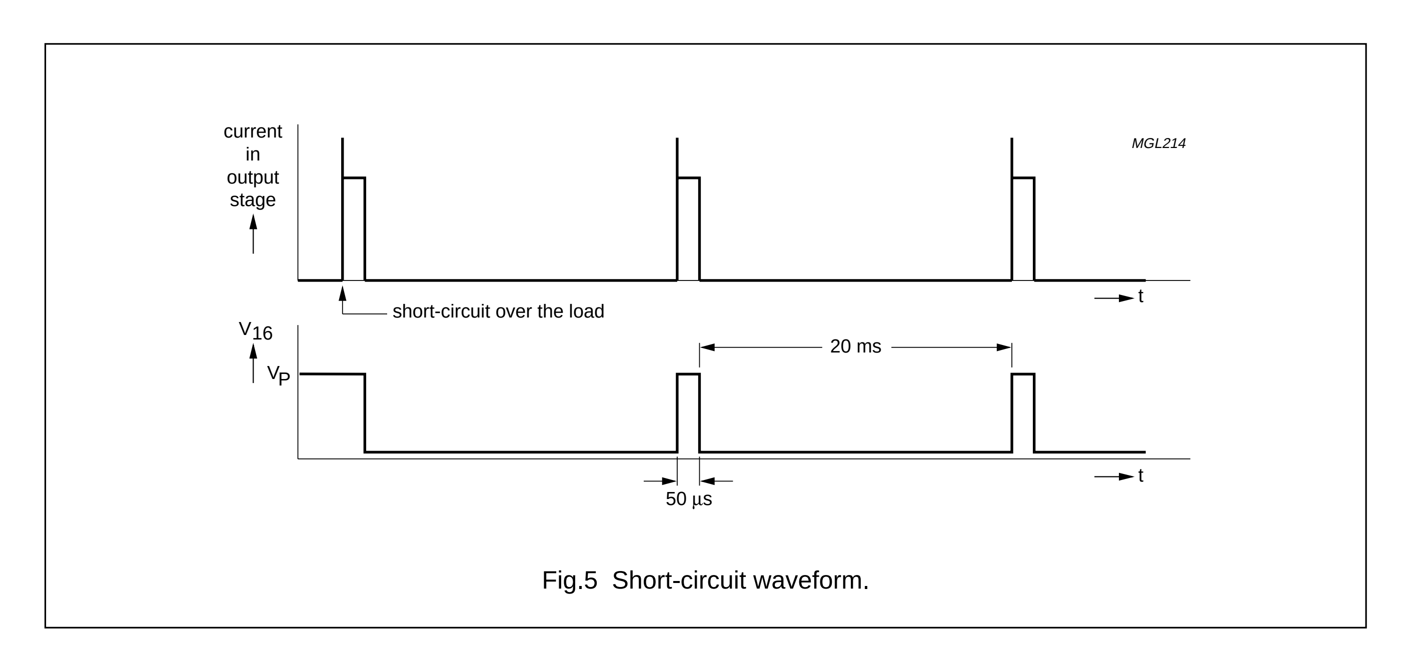


Fig.5 Short-circuit waveform.

TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 16 will be active LOW.

OPEN-COLLECTOR OUTPUT

Pin 16 is an open-collector output, which allows pin 16 of more devices being tied together.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

THERMAL CHARACTERISTICS

In accordance with IEC 747-1.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	40	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case (see Figs 6 and 7)	1.3	K/W

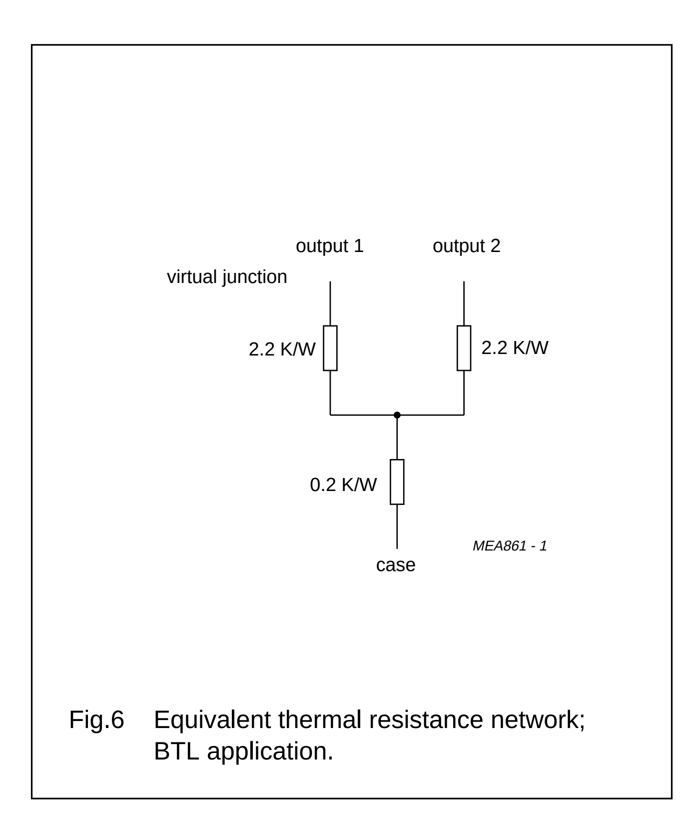


Fig.6 Equivalent thermal resistance network; BTL application.

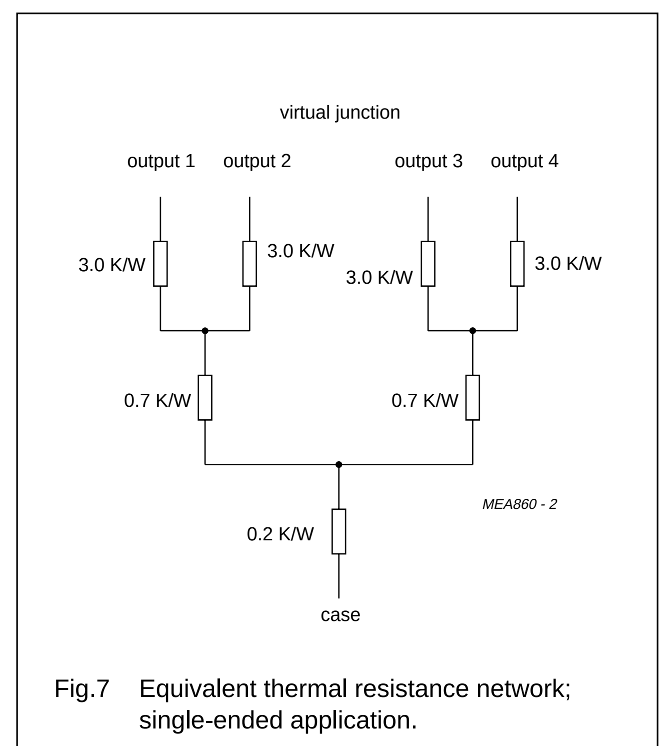


Fig.7 Equivalent thermal resistance network; single-ended application.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6	14.4	18	V
I_P	total quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
Mode select switch						
V_{on}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output voltage in mute position	V_{Imax} = 1 V; f = 1 kHz	–	–	2	mV
$\|\Delta V_O\|$	DC output offset voltage (between pins 6 to 8 and 10 to 12)		–	–	150	mV
STANDBY CONDITION						
V_{sb}	standby voltage		0	–	2	V
I_{sb}	standby current		–	–	100	μA
I_{sw}	switch-on current		–	12	40	μA
Diagnostic output (pin 16)						
V_{DIAG}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage $\leq 0.5V_P$.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (measured in Fig.8)						
P_o	output power	note 1				
		THD = 0.5%	15	19	–	W
		THD = 10%	20	24	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
P_o	output power	V_P = 13.2 V				
		THD = 0.5%	–	16	–	W
		THD = 10%	–	20	–	W
B	power bandwidth	THD = 0.5%; P_o = –1 dB; with respect to 15 W	–	20 to 15000	–	Hz
f_l	low frequency roll-off	at –1 dB; note 2	–	45	–	Hz
f_h	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	note 3				
	on		48	–	–	dB
	mute		48	–	–	dB
	standby		80	–	–	dB
$\lvert Z_I \rvert$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 4	–	70	–	μV
	on	R_s = 10 kΩ; note 4	–	100	200	μV
	mute	notes 4 and 5	–	60	–	μV
α_{cs}	channel separation	R_s = 10 kΩ	40	–	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_{16} \leq 0.6$ V; no short-circuit	–	10	–	%
Quad single-ended application (measured in Fig.9)						
P_o	output power	note 1				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	7	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
P_O	output power	R_L = 2 Ω; note 1				
		THD = 0.5%	7.5	10	–	W
		THD = 10%	10	12	–	W
f_l	low frequency roll-off	at –1 dB; note 2	–	25	–	Hz
f_h	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	note 3				
	on		48	–	–	dB
	mute		48	–	–	dB
	standby		80	–	–	dB
$\|Z_I\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 4	–	50	–	μV
	on	R_s = 10 kΩ; note 4	–	70	100	μV
	mute	notes 4 and 5	–	50	–	μV
α_{cs}	channel separation	R_s = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_{16} \leq 0.6$ V; no short-circuit	–	10	–	%

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p) and at a frequency of between 100 Hz and 10 kHz.
4. Noise measured in a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage independent of R_s (V_i = 0 V).

TEST AND APPLICATION INFORMATION

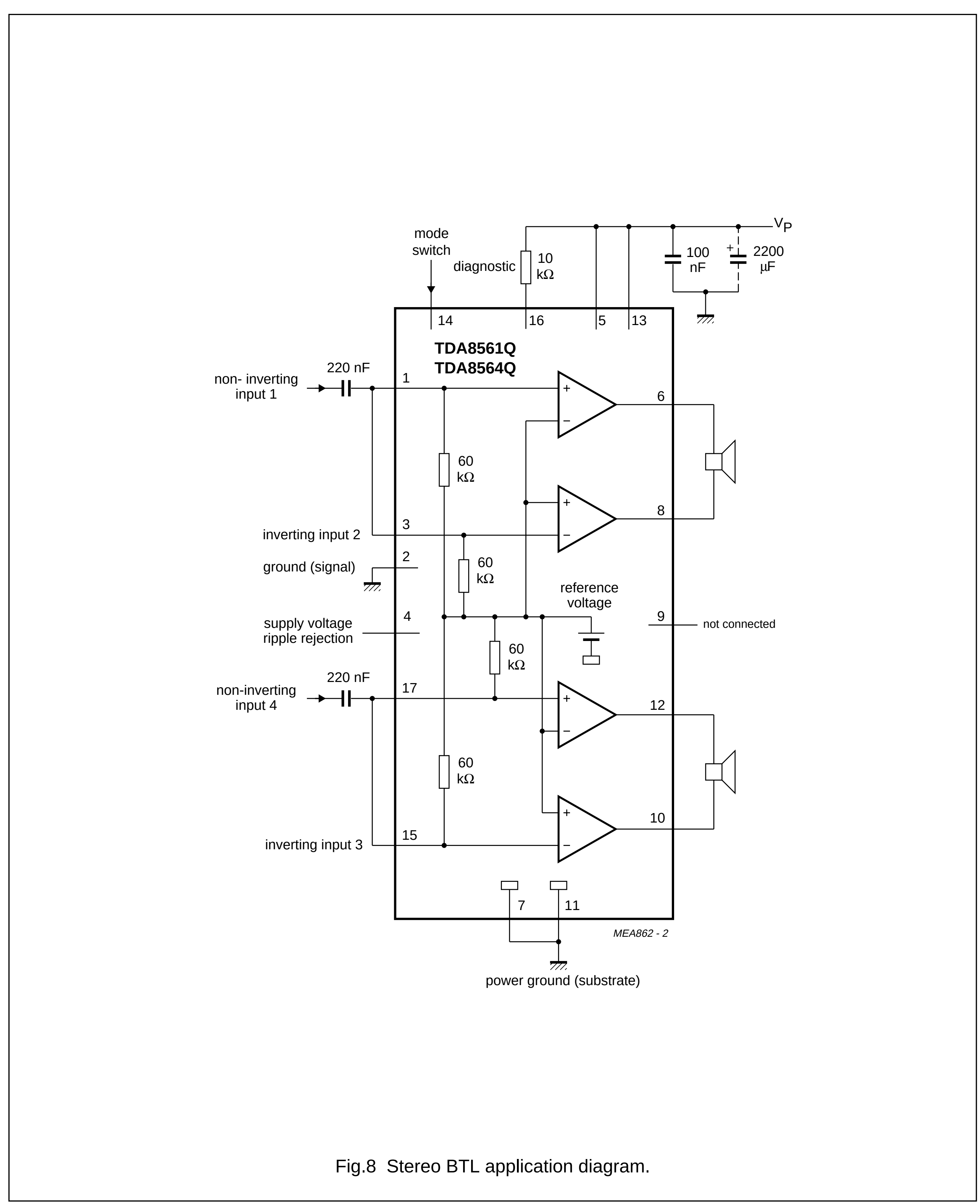


Fig.8 Stereo BTL application diagram.

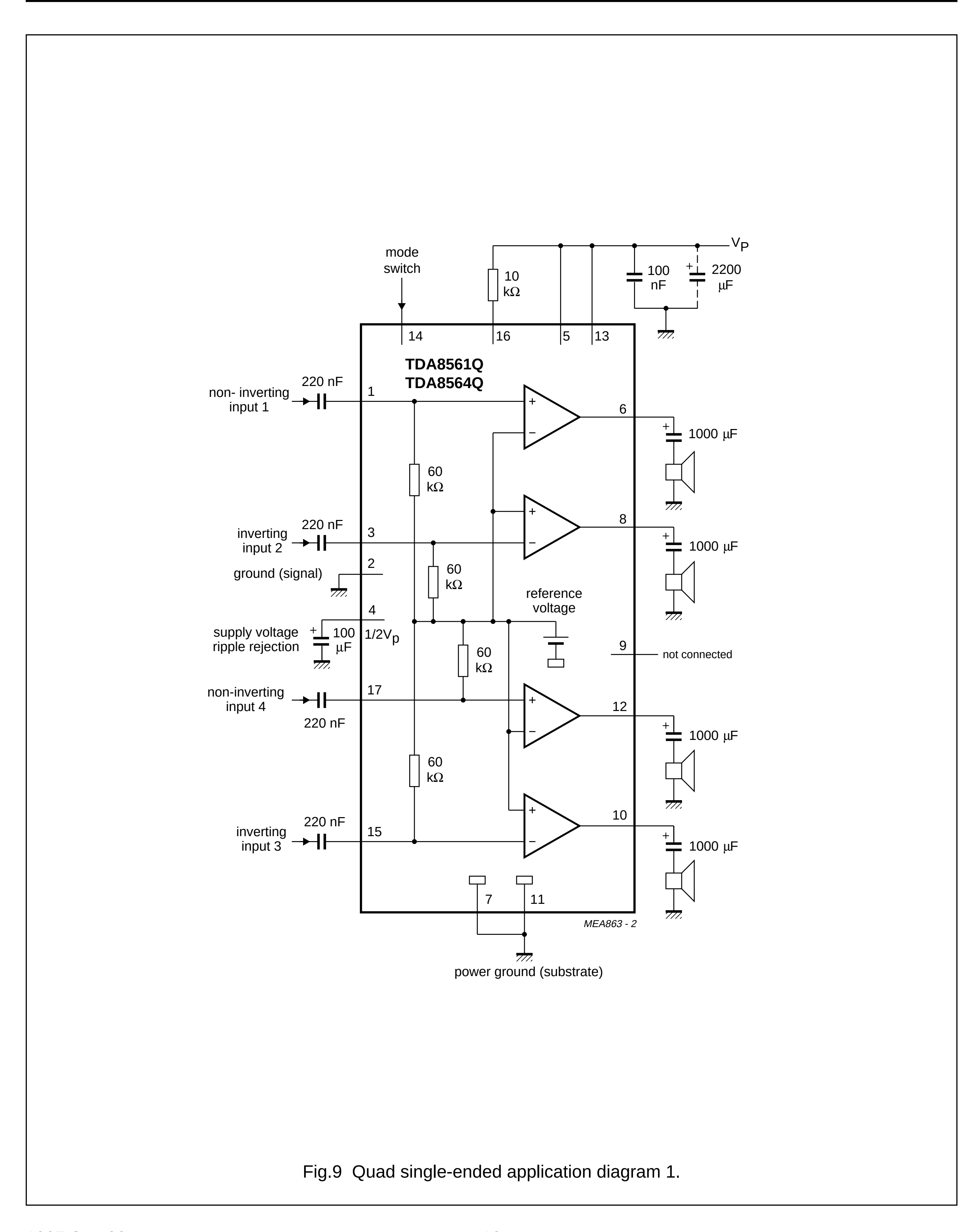
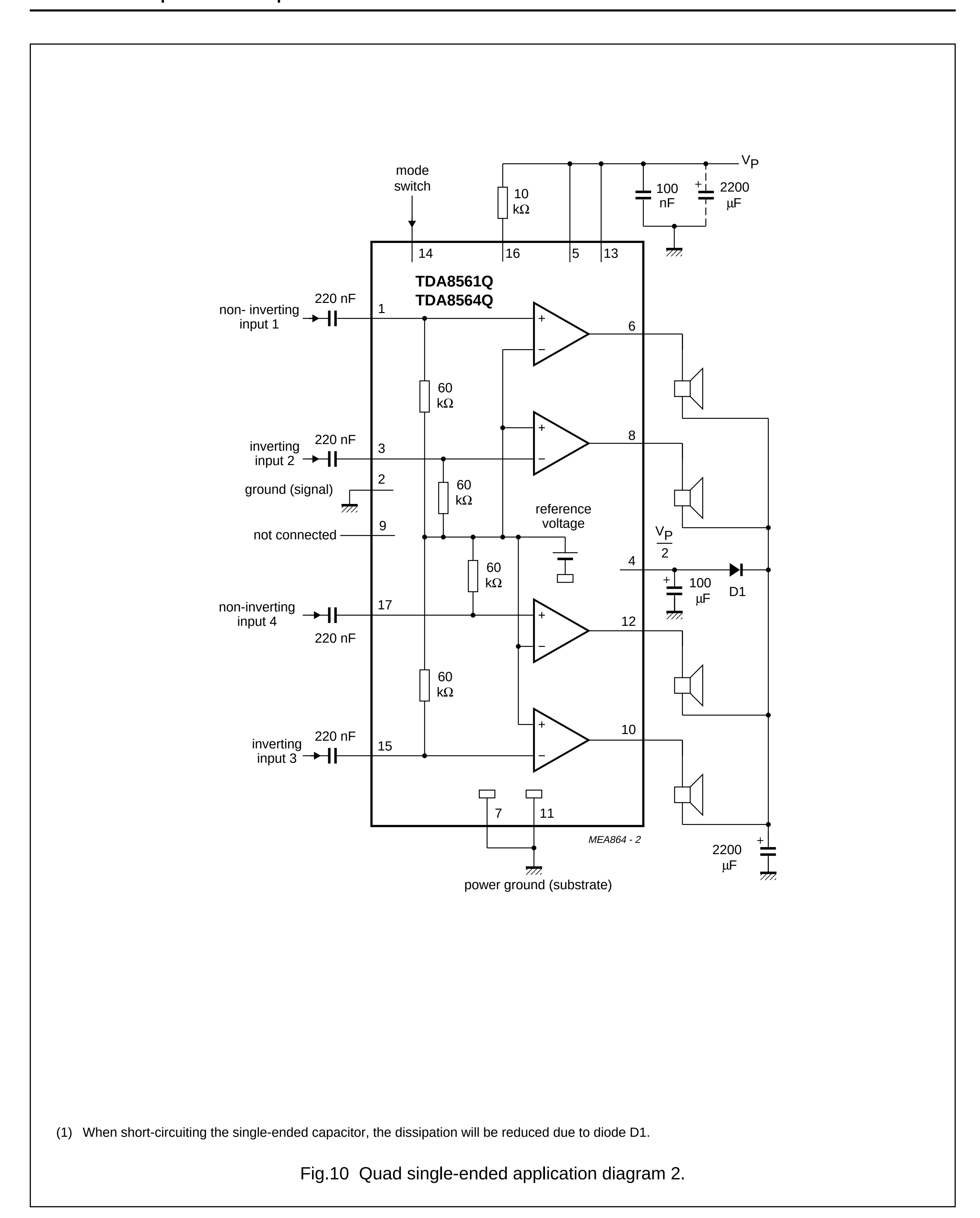


Fig.9 Quad single-ended application diagram 1.



(1) When short-circuiting the single-ended capacitor, the dissipation will be reduced due to diode D1.

Fig.10 Quad single-ended application diagram 2.

Mode select switch

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during >100 ms (charging of the input capacitors at pins 1, 3, 15 and 17.

The circuit in Fig.11 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

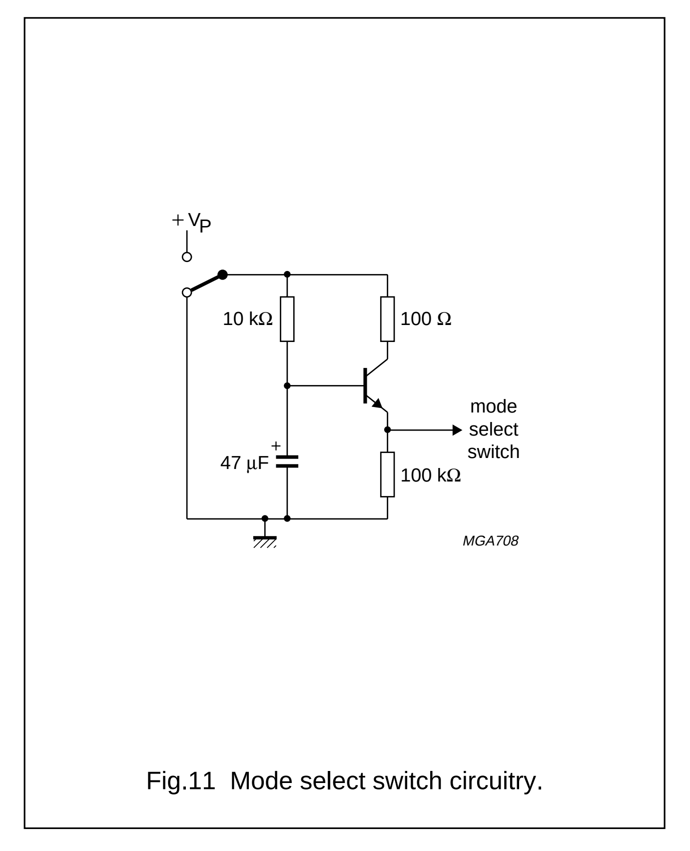


Fig.11 Mode select switch circuitry.

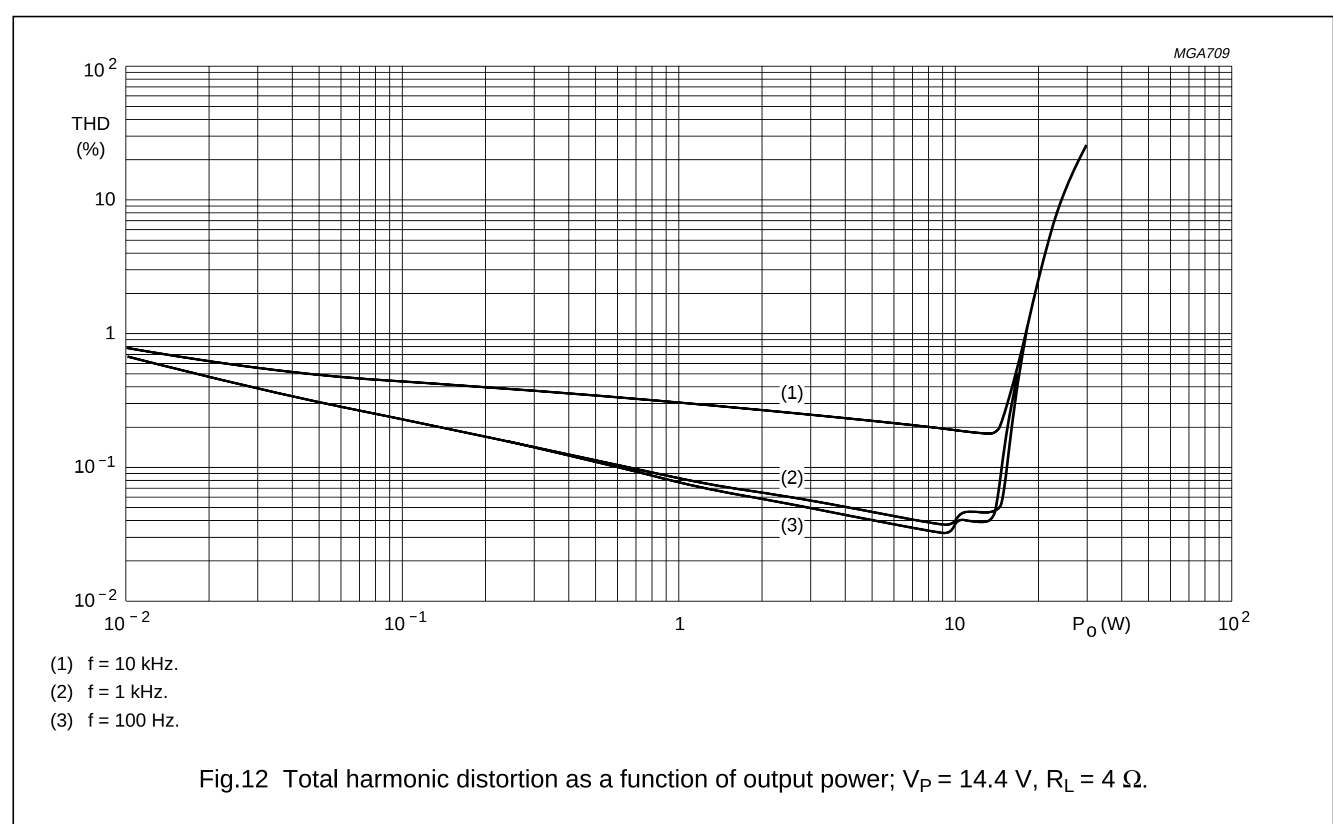
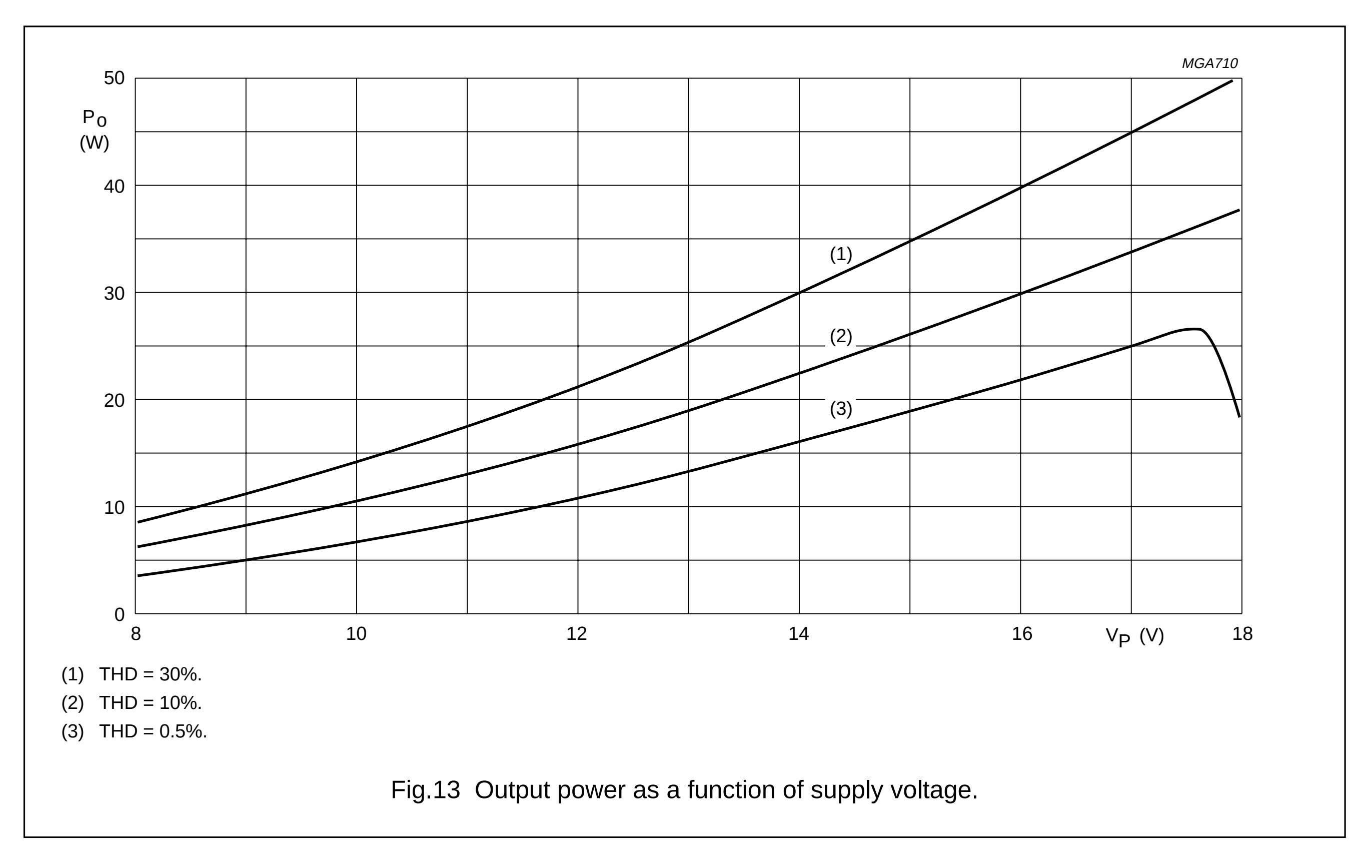


Fig.12 Total harmonic distortion as a function of output power; V_P = 14.4 V, R_L = 4 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.13 Output power as a function of supply voltage.

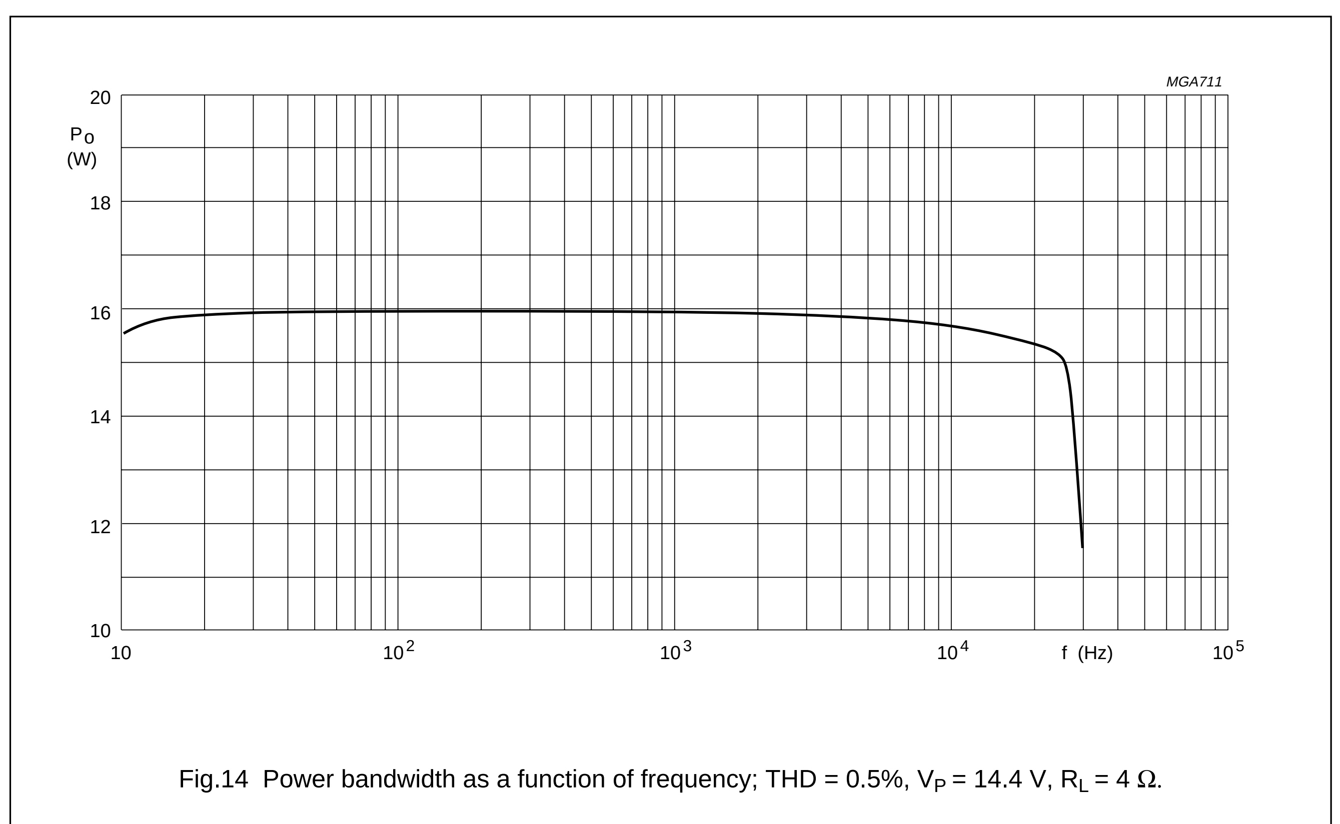
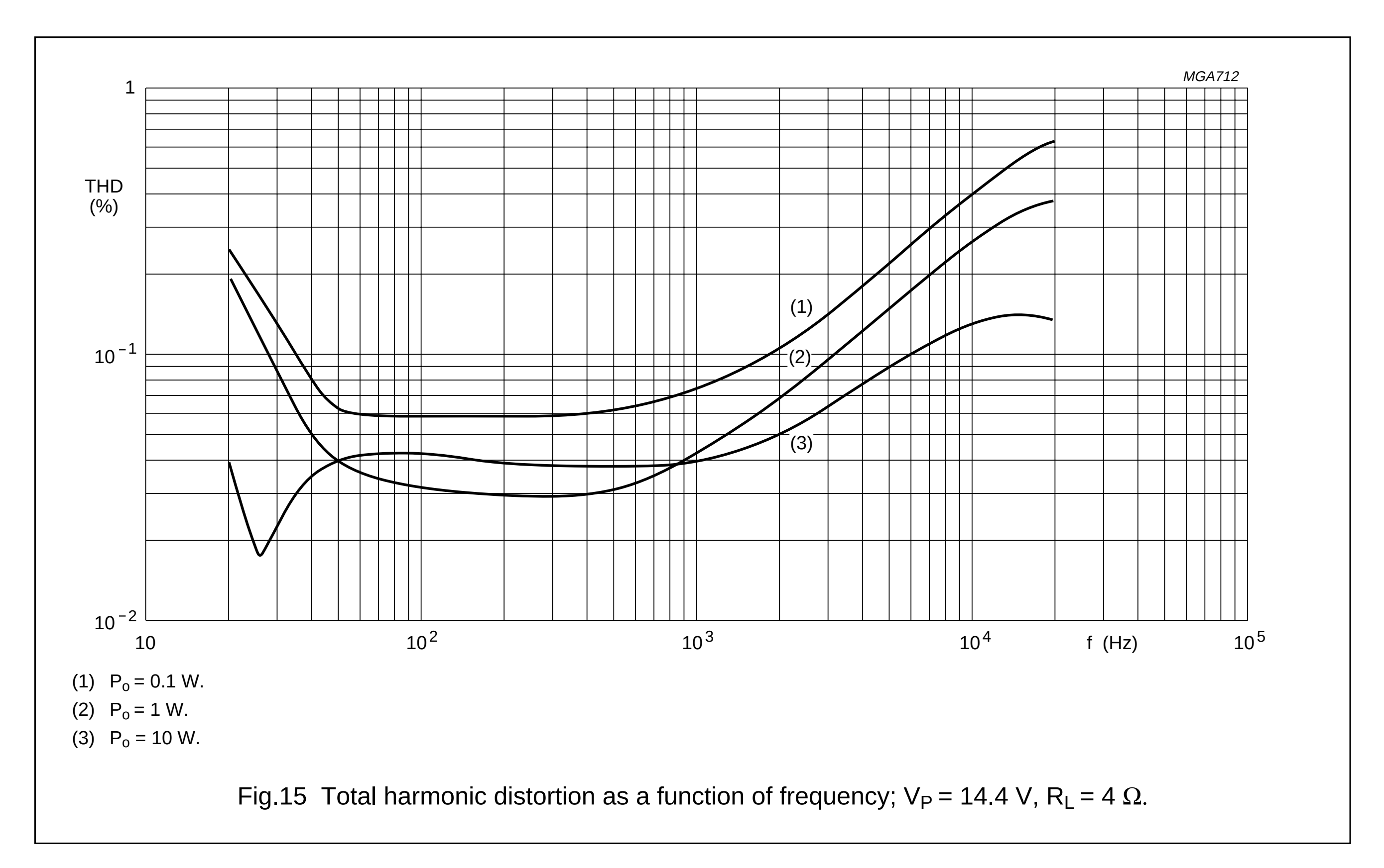
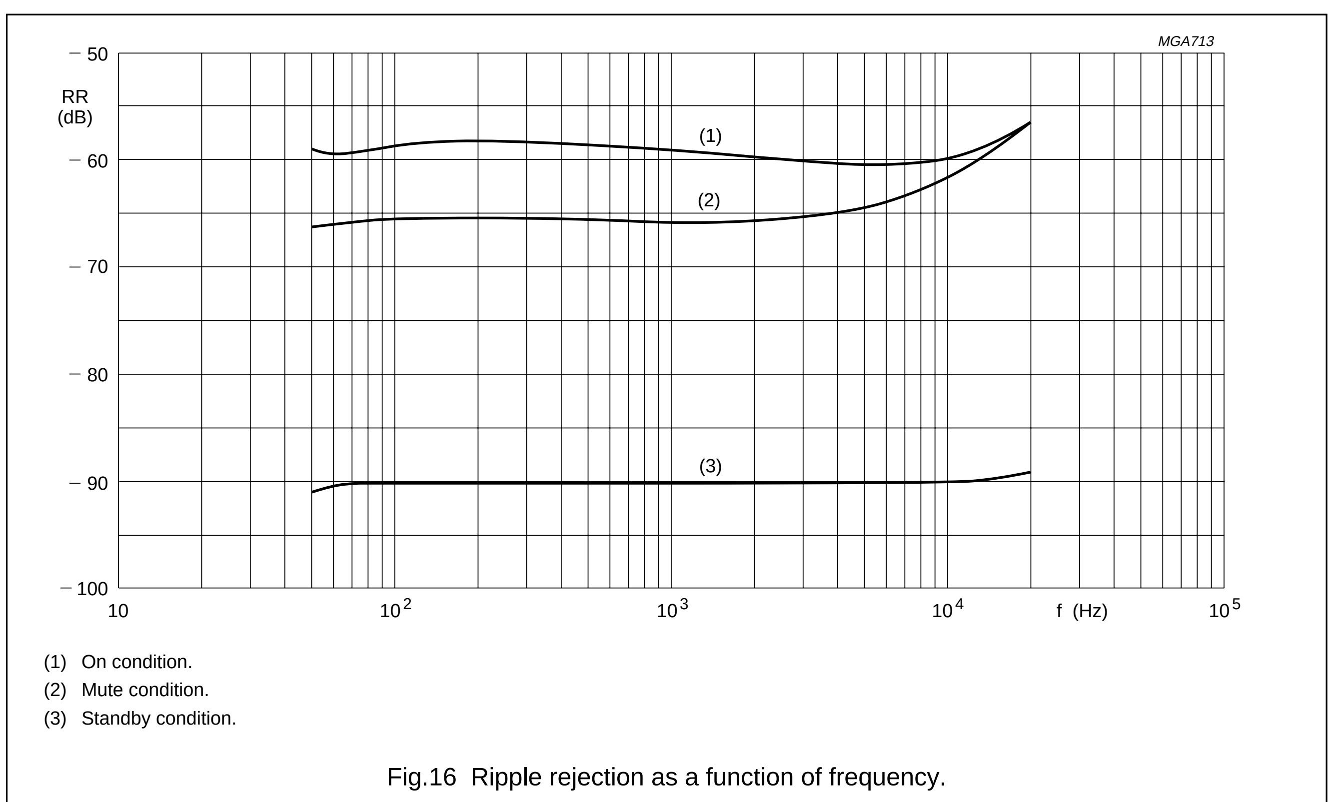


Fig.14 Power bandwidth as a function of frequency; THD = 0.5%, V_P = 14.4 V, R_L = 4 Ω.



(1) P_o = 0.1 W.
(2) P_o = 1 W.
(3) P_o = 10 W.

Fig.15 Total harmonic distortion as a function of frequency; V_P = 14.4 V, R_L = 4 Ω.



(1) On condition.
(2) Mute condition.
(3) Standby condition.

Fig.16 Ripple rejection as a function of frequency.

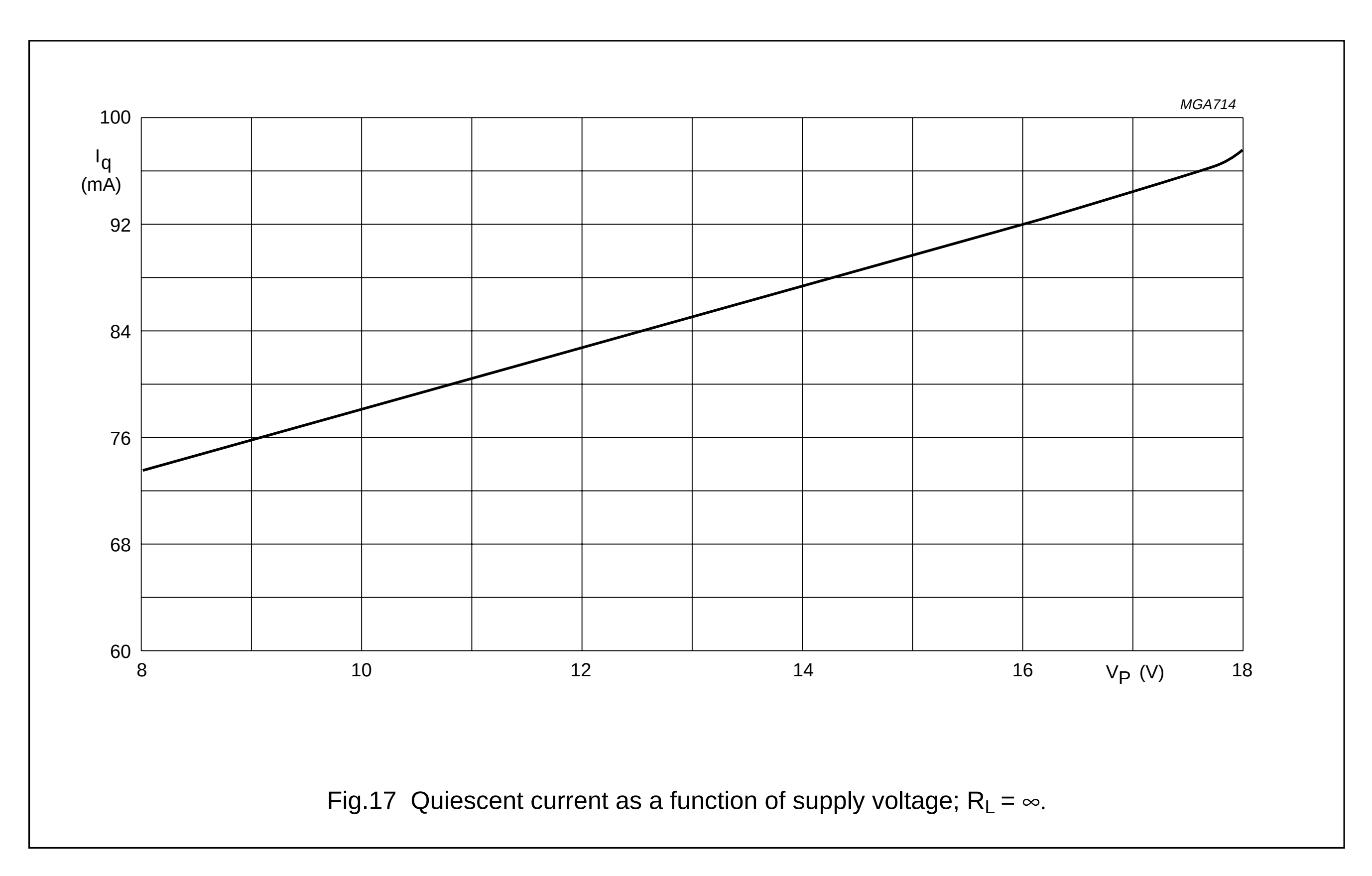
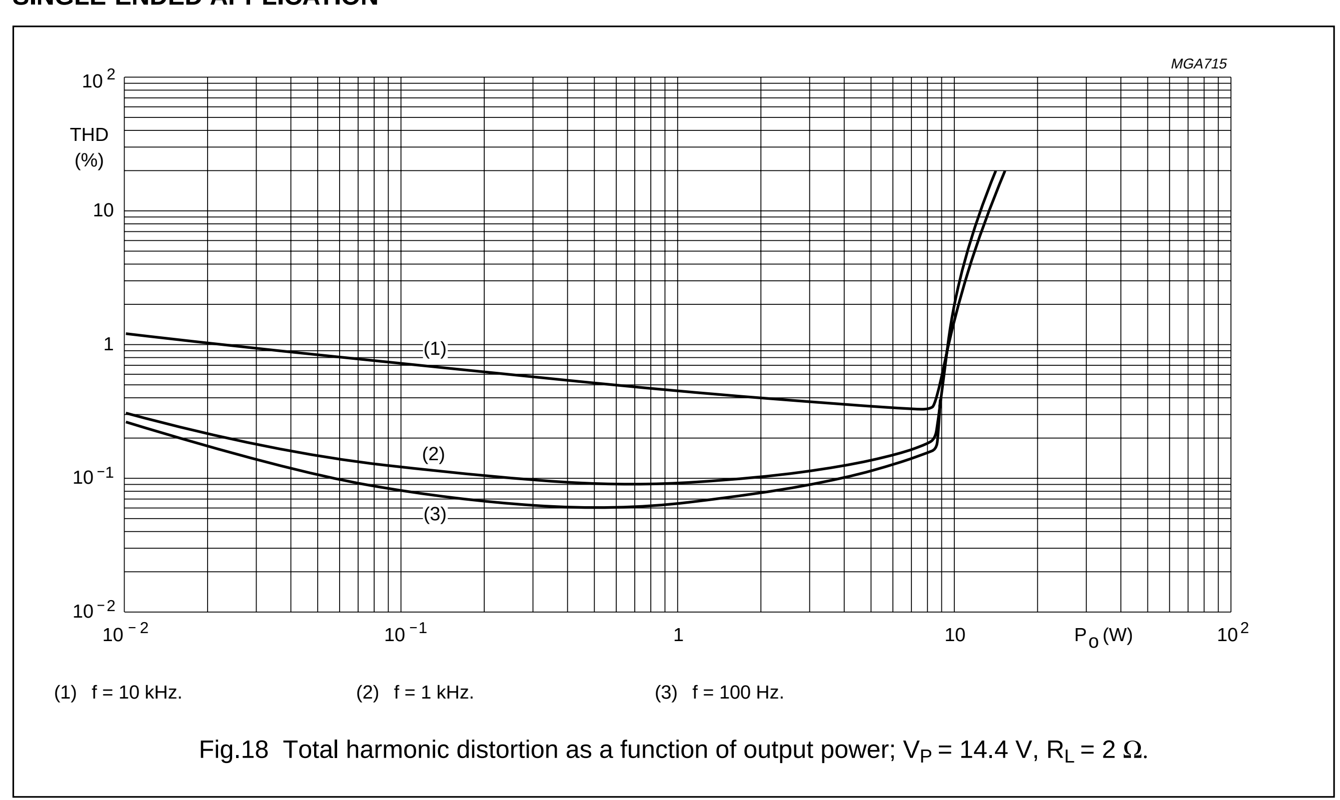


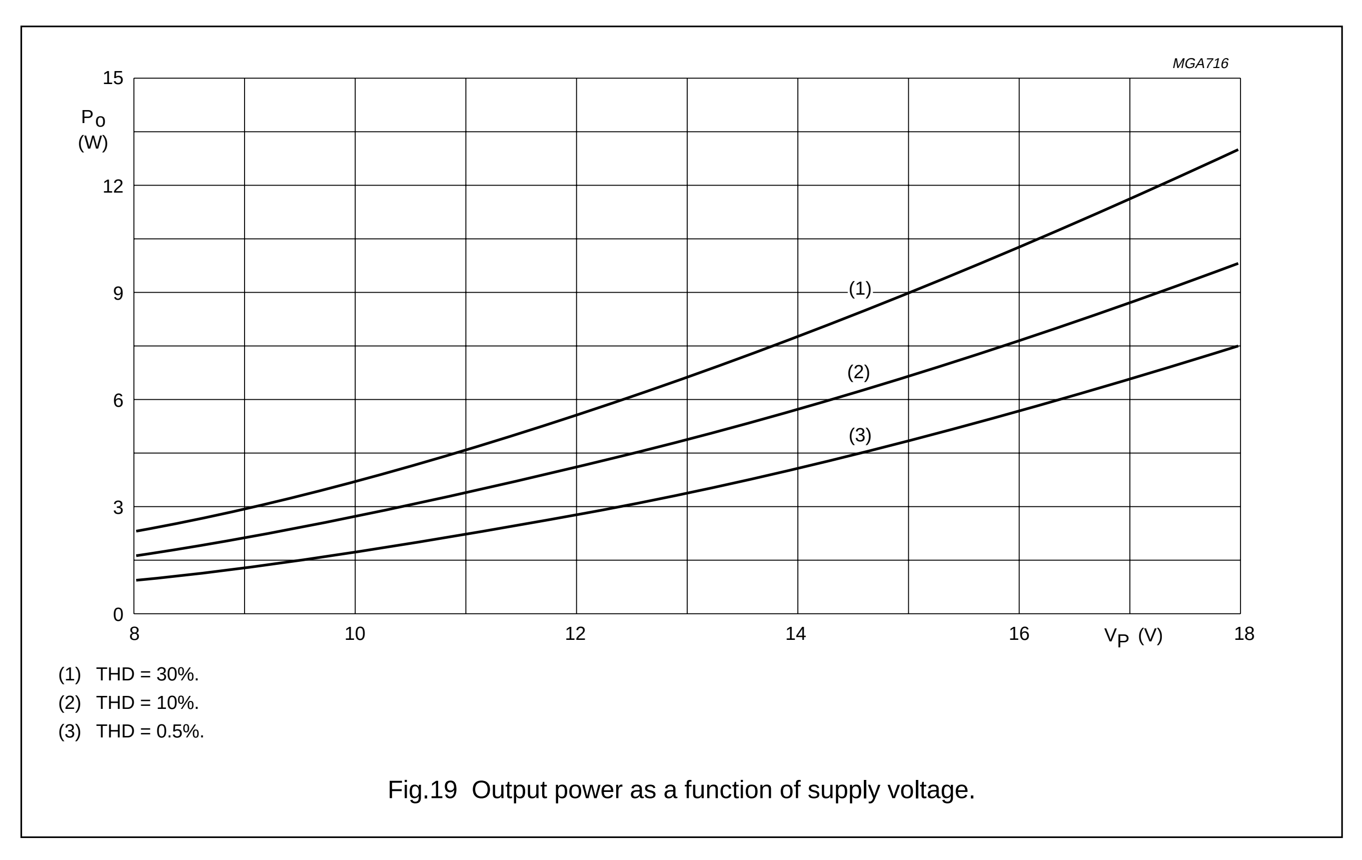
Fig.17 Quiescent current as a function of supply voltage; $R_L = \infty$.

SINGLE-ENDED APPLICATION



(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.18 Total harmonic distortion as a function of output power; V_P = 14.4 V, R_L = 2 Ω.



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.19 Output power as a function of supply voltage.

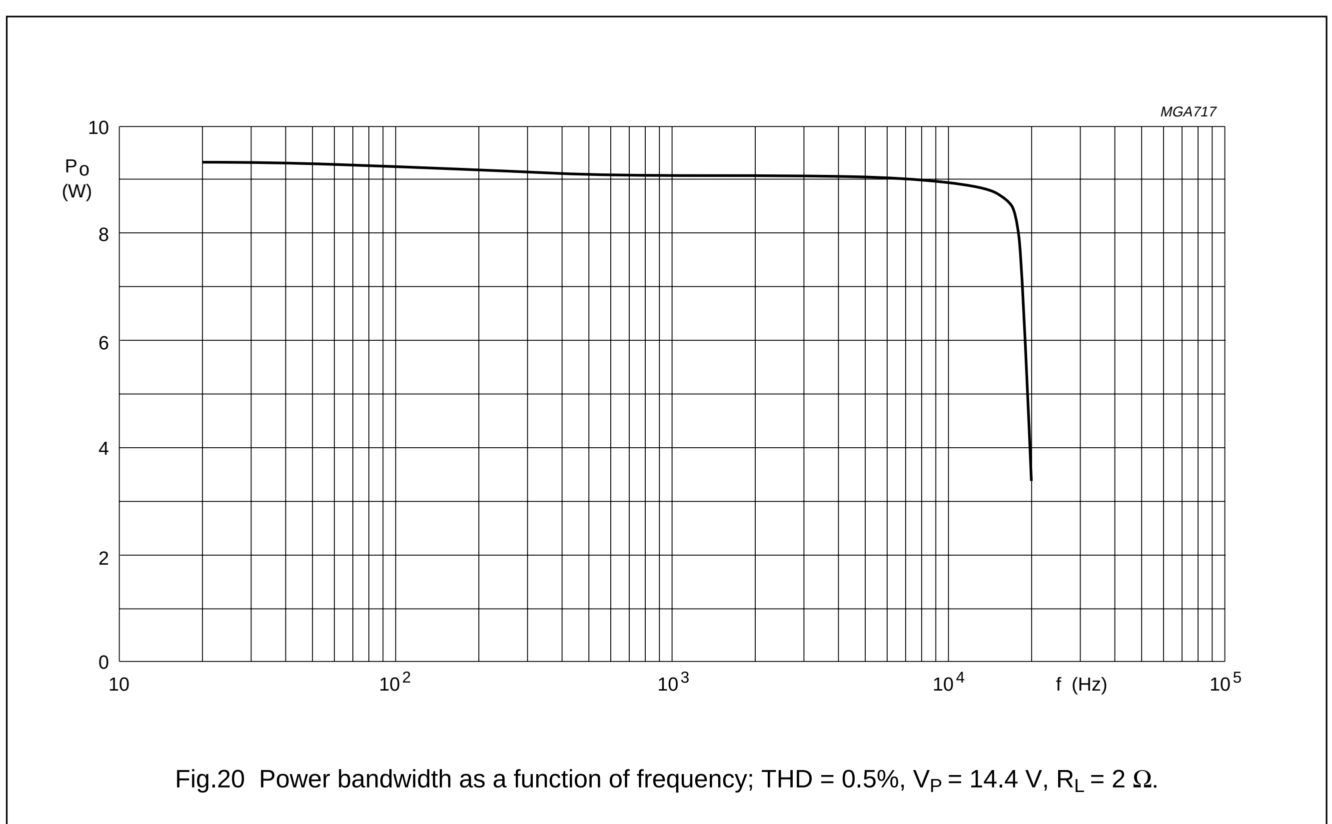


Fig.20 Power bandwidth as a function of frequency; THD = 0.5%, V_P = 14.4 V, R_L = 2 Ω.

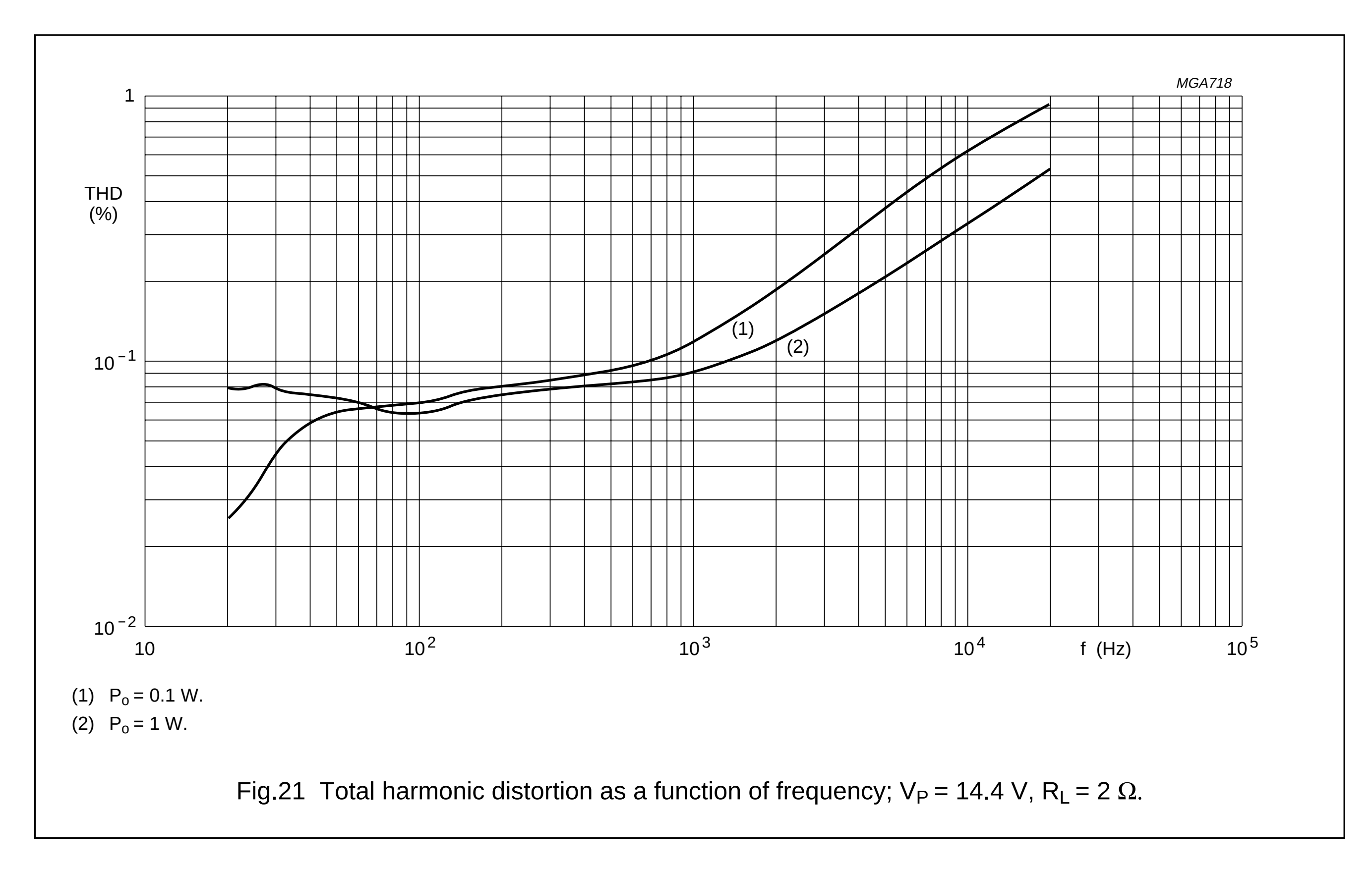


Fig.21 Total harmonic distortion as a function of frequency; V_P = 14.4 V, R_L = 2 Ω.

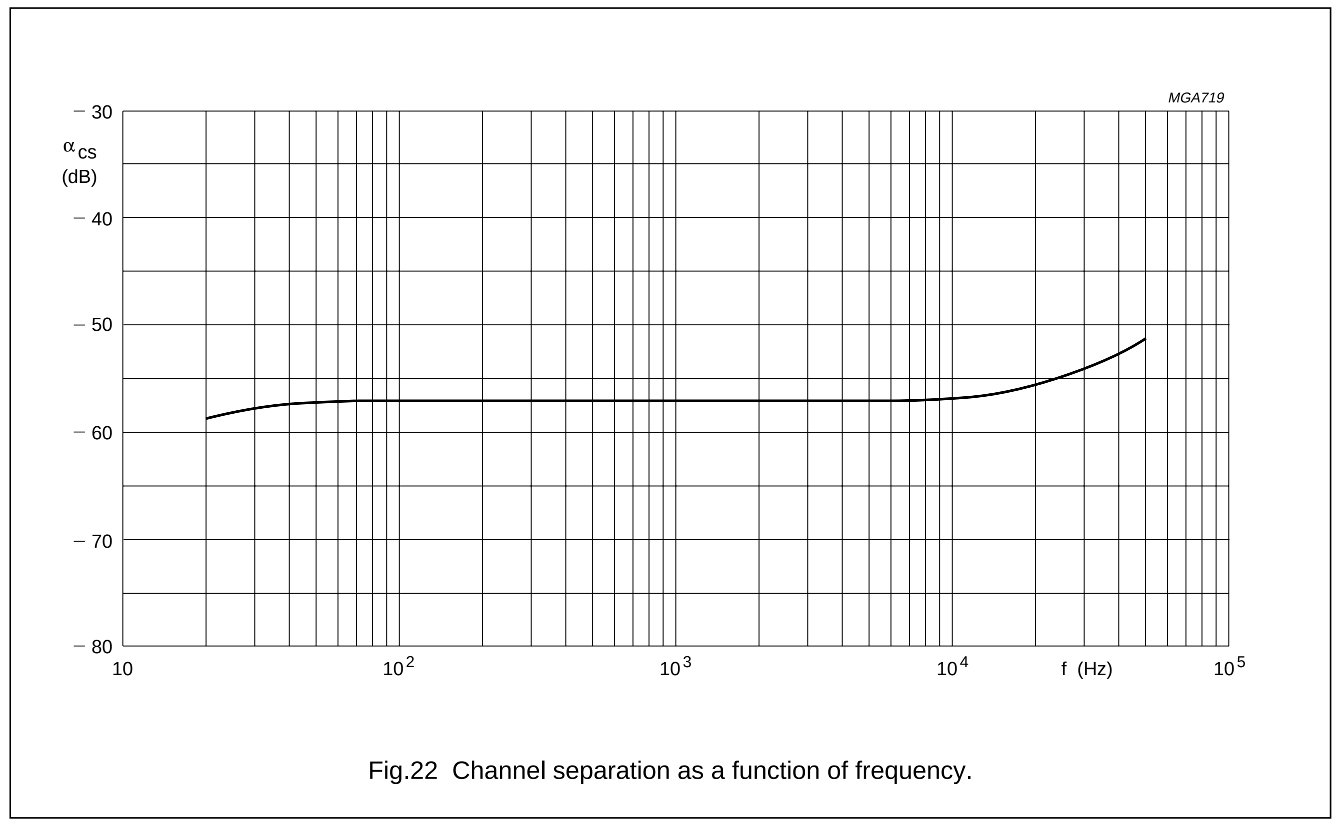


Fig.22 Channel separation as a function of frequency.

BTL APPLICATION

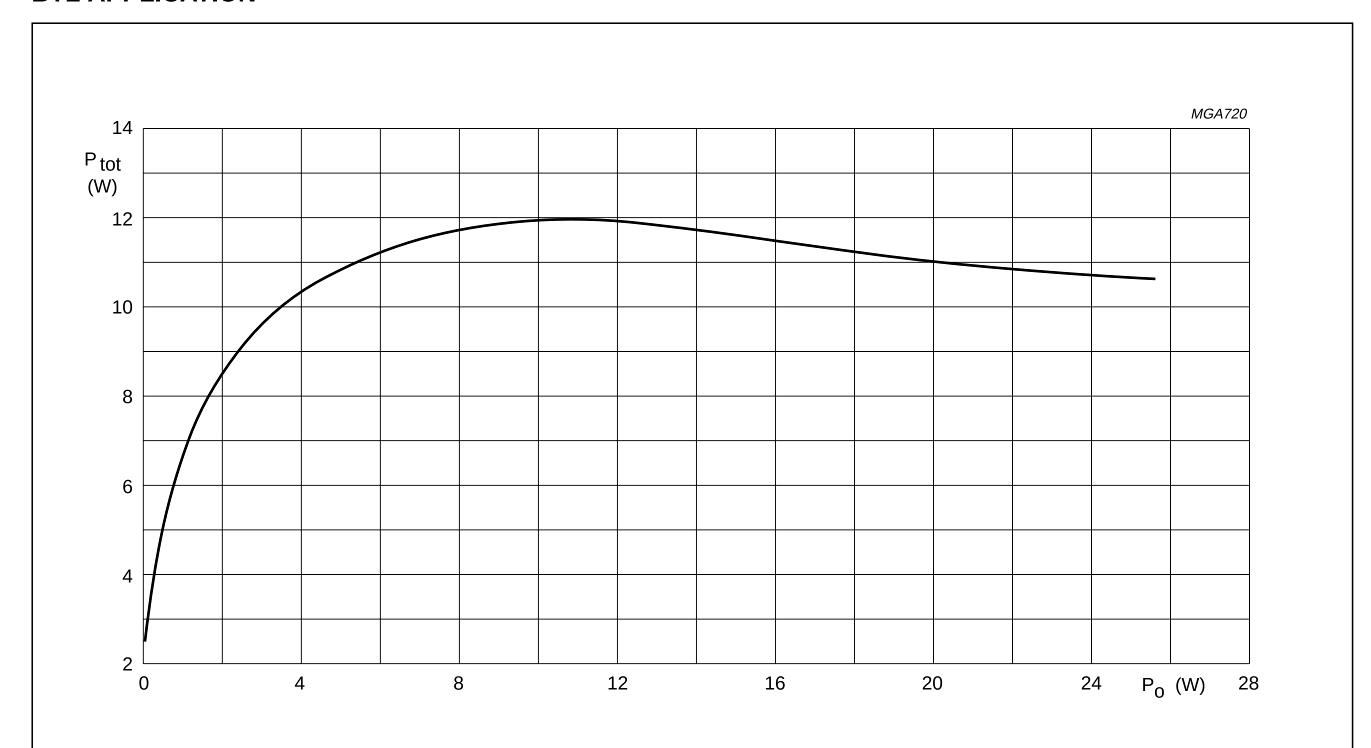
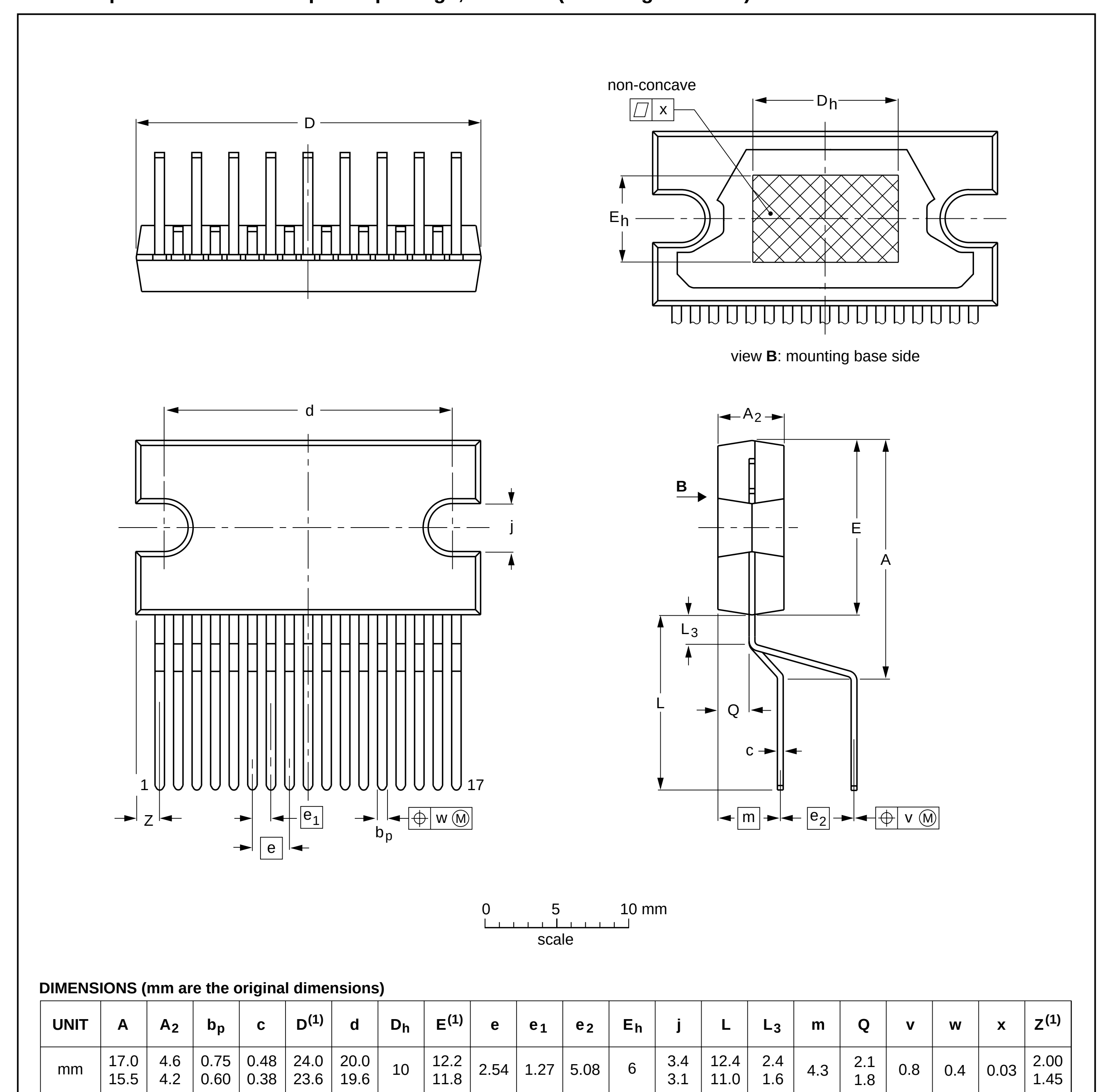


Fig.23 Total power dissipation as a function of output power; V_P = 14.4 V, R_L = 4 Ω (1 channel driven BTL or 4 channels in single-ended mode).

PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Argentina: see South America
Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466
Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010, Fax. +43 160 101 1210
Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773
Belgium: see The Netherlands
Brazil: see South America
Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102
Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381
China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700
Colombia: see South America
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Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 0044
Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920
France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427
Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300
Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240
Hungary: see Austria
India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966
Indonesia: see Singapore
Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200
Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007
Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557
Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077
Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415
Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880
Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381
Middle East: see Italy
Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399
New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811
Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341
Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474
Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327
Portugal: see Spain
Romania: see Italy
Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919
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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494
South America: Rua do Rocio 220, 5th floor, Suite 51, 04552-903 São Paulo, SÃO PAULO - SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 829 1849
Spain: Balmes 22, 08007 BARCELONA, Tel. +34 3 301 6312, Fax. +34 3 301 4107
Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 632 2000, Fax. +46 8 632 2745
Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2686, Fax. +41 1 481 7730
Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874
Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793
Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707
Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461
United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421
United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381
Uruguay: see South America
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Printed in The Netherlands 547027/1200/03/pp24 Date of release: 1997 Sep 22 Document order number: 9397 750 02866

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